FROM RESEARCH TO INDUSTRY

cea tech

DISSIPATION IN INTEGRATED CIRCUITS AND ADIABATIC SOLUTIONS

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leti

- Limits of CMOS
- Adiabatic Solutions
- Capacitor Based Adiabatic Solutions

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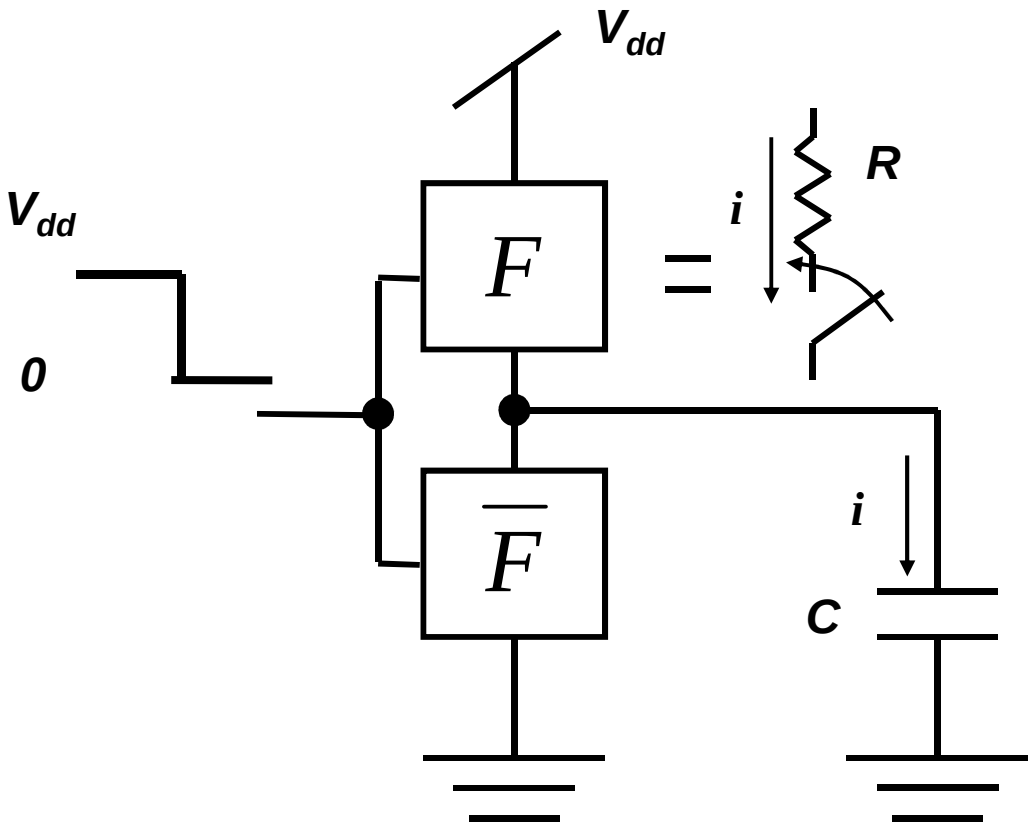
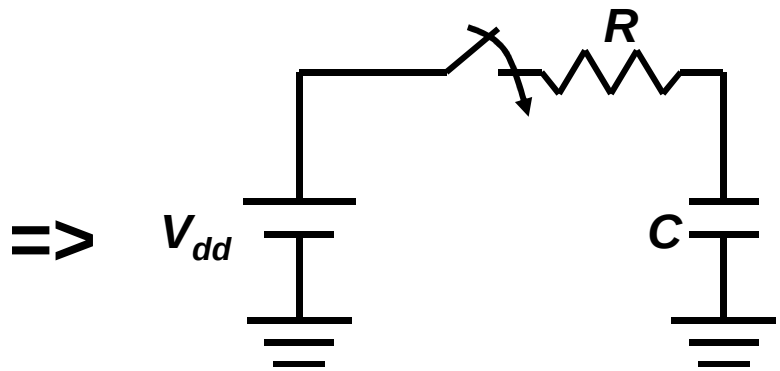
More Performance… Less Power

J. Rabaey, *ASPDAC* 2008

4



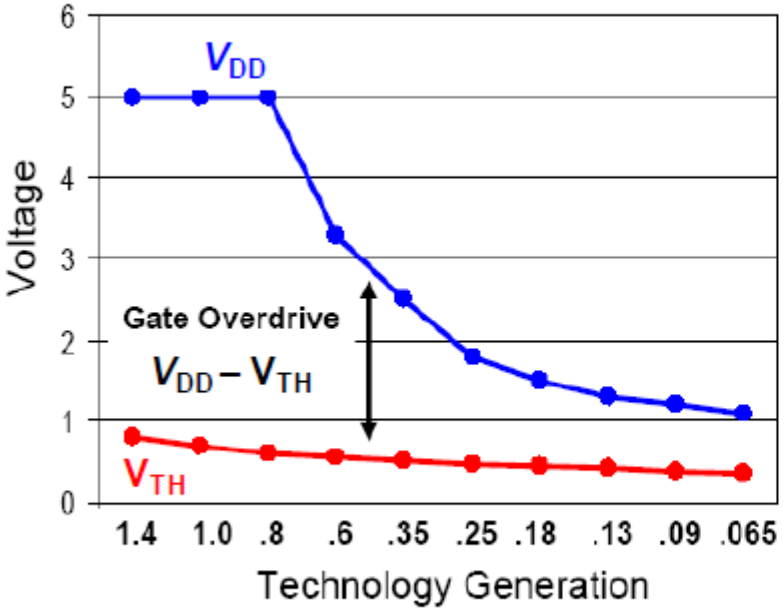


$$E_{active} = \frac{1}{2} C V_{dd}^2$$

$$E_{leakage} = V_{DD} I_{leak} T$$

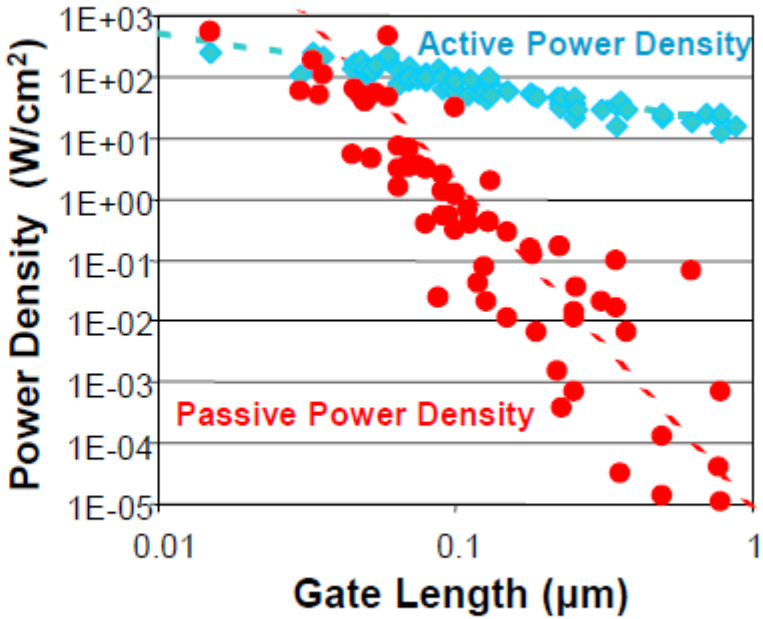
5

CMOS Voltage Scaling



Source: P. Packan (Intel),
2007 IEDM Short Course

Power Density vs. Gate Length



Source: B. Meyerson (IBM)
Semico Conf., January 2004

CMOS LIMITS

$$E = \alpha \cdot N \cdot C \cdot k^2 \cdot n^2 \cdot v_t^{\,2} \frac{1}{(1-k\eta)^2}\left(y^2 + my \cdot e^{-y}\right)$$

$f(y)$

Normalized threshold

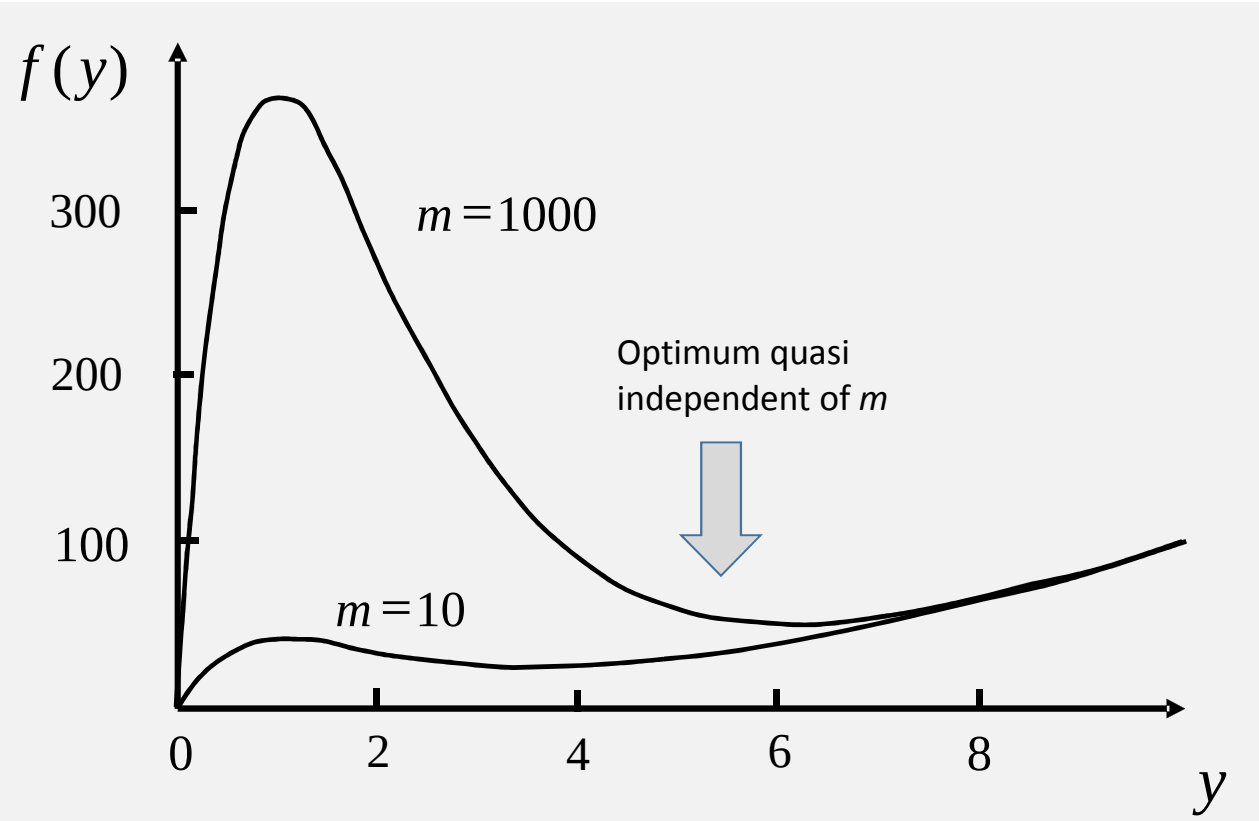
$$y = V_T(1-k\eta) \;/nv_t$$

Overdrive factor

$$k = \frac{V_{DD}}{V_T}$$

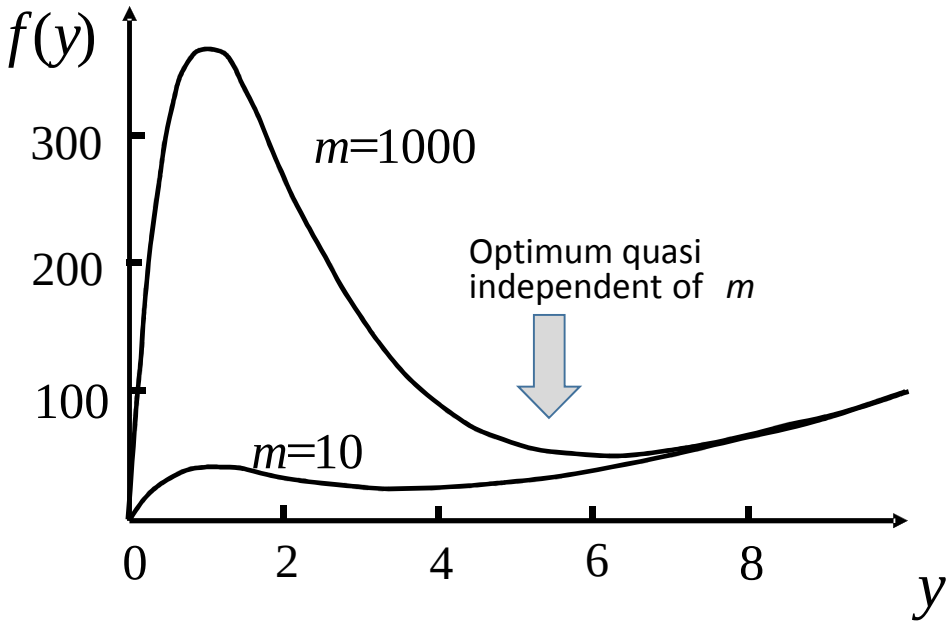
Technology and architecture dependent parameter

$$m = \frac{Tv_t}{\alpha nk} \cdot \frac{WC_{OX}}{LC} \mu \cdot e^{1.8} \cdot (1-k\eta)$$



***V_T* optimal around 200 mV independently of technology and architecture**

CMOS LIMITS

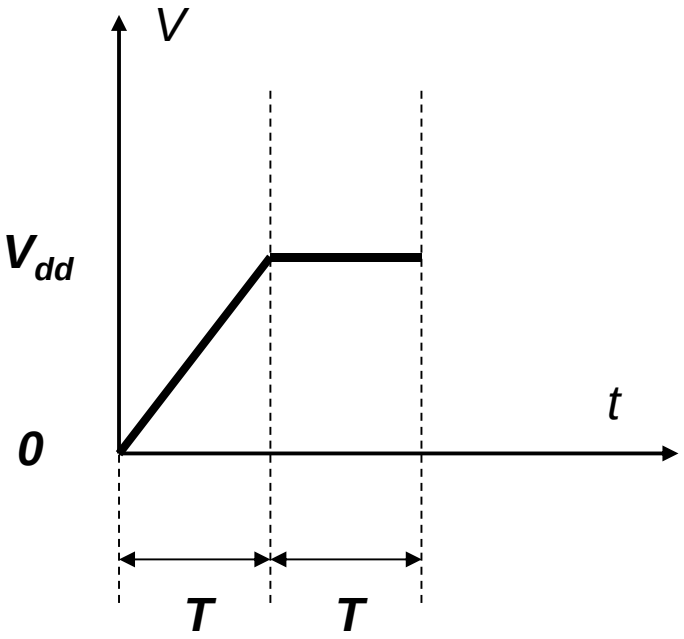


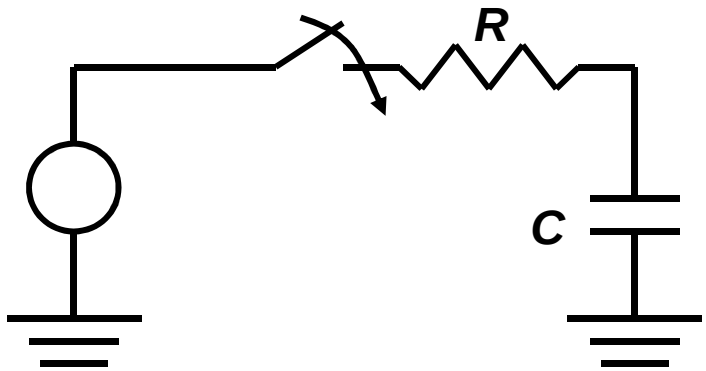
V_T optimal around 200 mV independently of technology and architecture

V_{DD} optimal around 600 mV for high performance regime
V_{DD} optimal around 400 mV for near-threshold regime
V_{DD} optimal around 250 mV for sub-threshold regime

No solution for ultra low power with CMOS

- Limits of CMOS
- Adiabatic Solutions
- Capacitor Based Adiabatic Solutions

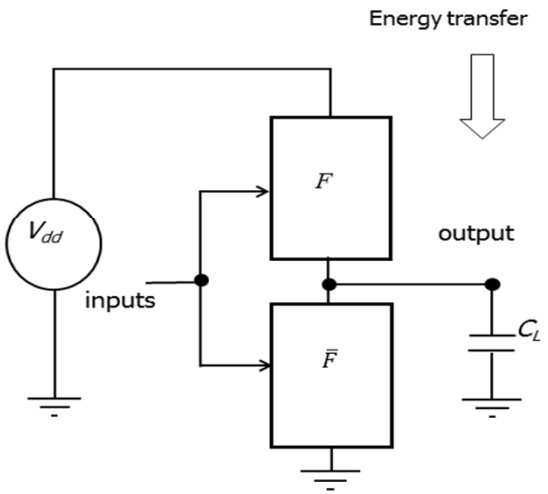




$$E_{adiabatic} \cong \frac{RC}{T} CV_{dd}^{\ 2}$$

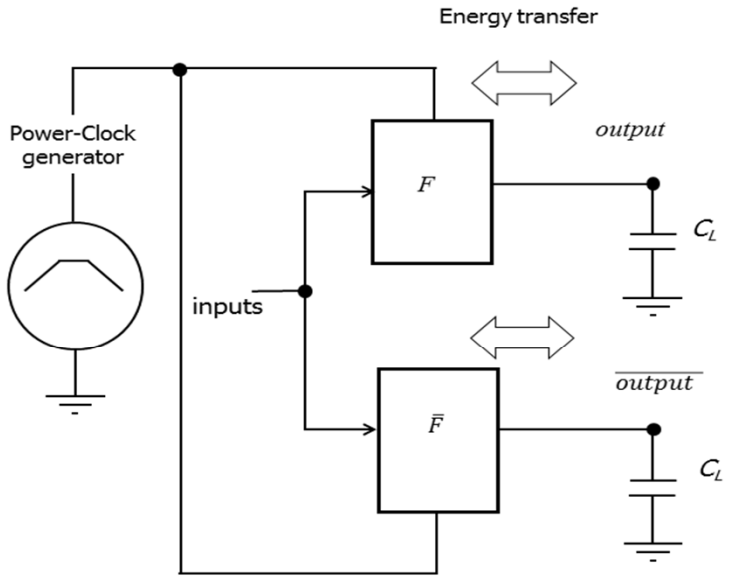
10

V_{DD} constant



Conventional Logic

V_{DD} not constant



Adiabatic Logic

$$E = CV_{DD}^{\ 2} + leakage$$

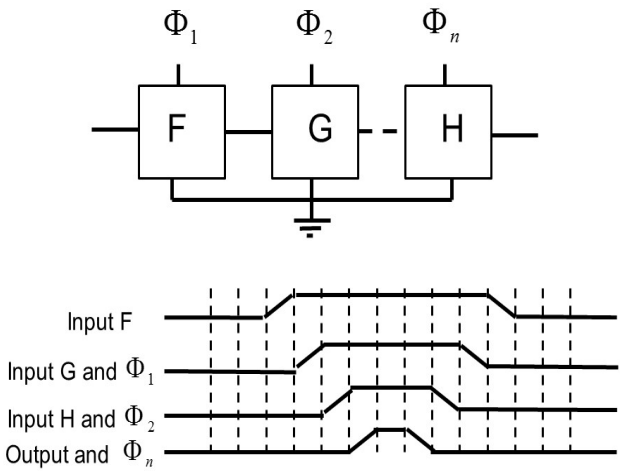
$$E = \frac{2RC}{T} CV_{DD}^{\ 2} + leakage$$

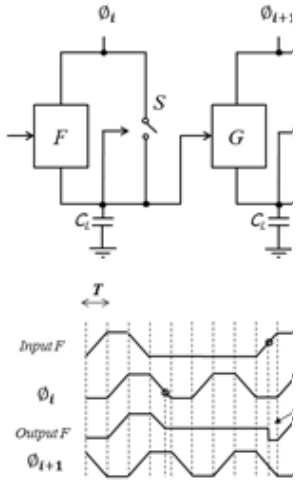
BUT INPUTS HAVE TO BE STABLE DURING RAMP-UP AND RAMP-DOWN

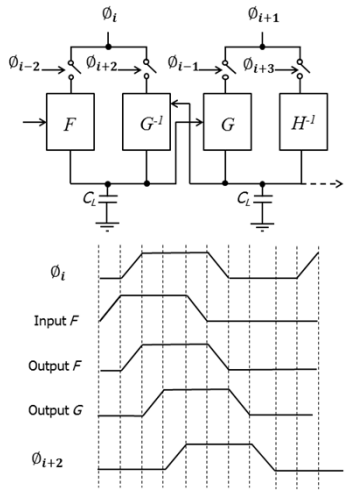
ULTRA LOW POWER SOLUTIONS

Optimal (for dissipation)charge and discharge of capacitances : the adiabatic mode

- Retractable logic solution
- Quasi-adiabatic pipeline
- Reversible pipeline





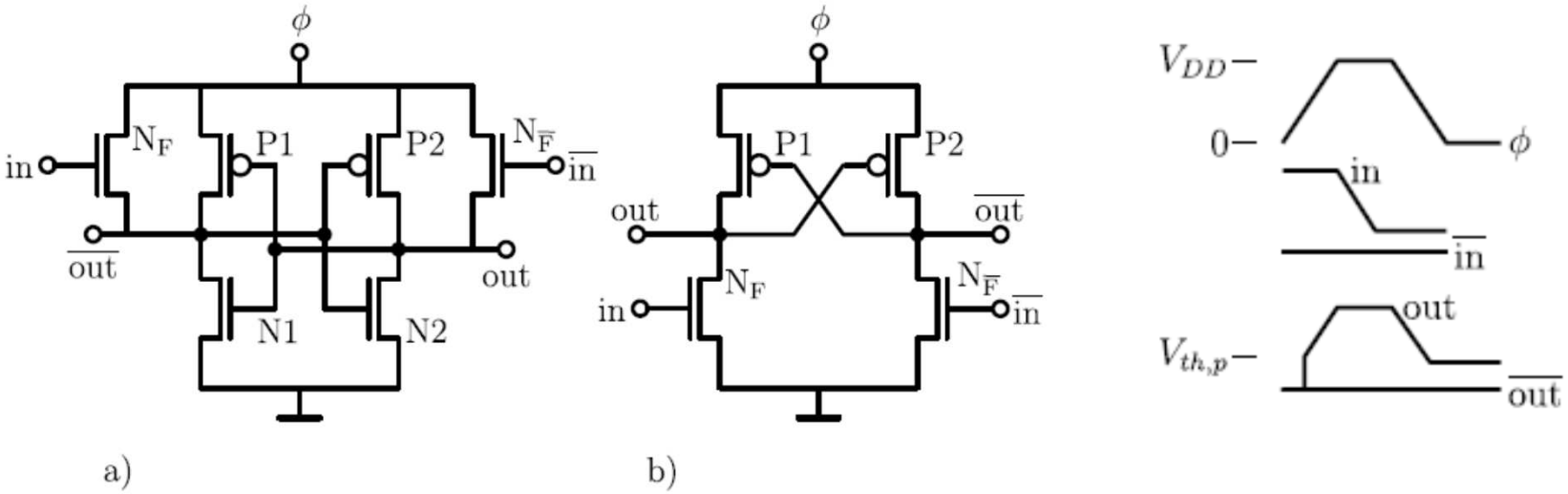


$$\text{CMOS}: \frac{RC}{T} CV_{DD}^{\ 2} + leakage$$

$$\text{CMOS}: CV_T^{\ 2} + \frac{RC}{T} CV_{DD}^{\ 2} + leakage$$

$$\text{CMOS}: \frac{RC}{T} CV_{DD}^{\ 2} + leakage$$

P. Teichmann, 2012



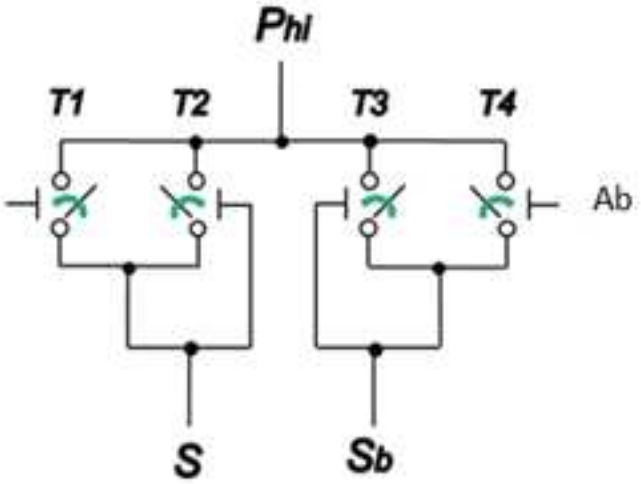
Inverter circuit in the (**a**) PFAL and (**b**) ECRL family

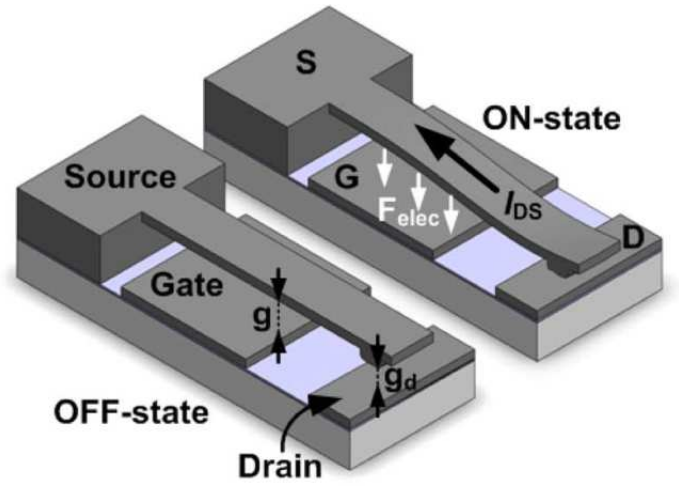
Adiabatic

Non-Adiabatic

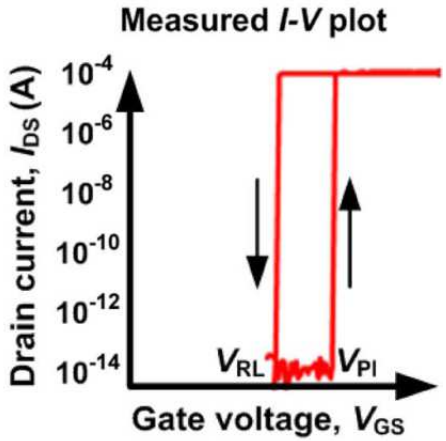
Leakage

$$E_{dissipated} \cong 2\frac{RC}{T}CV_{dd}{}^2 + \frac{1}{2}CV_T^2 + I_{leakage}V_{dd}T$$





(a)



(b)

$$E = 2\frac{R \cdot C_L}{T} C_L \cdot V_{dd}{}^2 + \frac{1}{2} C_L \cdot V_{RL}{}^2$$

NEMS CMOS COMPARISON

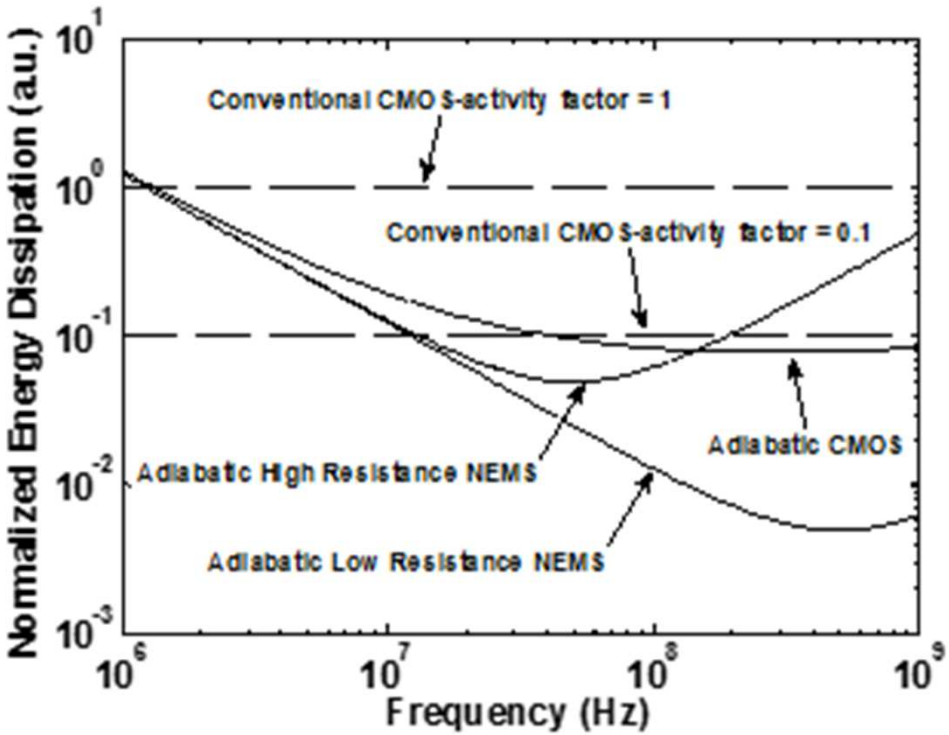
CMOS

$$E_{dissipated} \cong 2\frac{R_{cmos}C_L}{T}C_L{V_{dd}}^2 + \frac{1}{2}C_L V_T^2 + I_{leakage}V_{dd}T$$

NEMS

$$E_{dissipated} = 2\frac{R_{nems}\cdot C_L}{T}C_L\cdot{V_{dd}}^2 + \frac{1}{2}C_L\cdot{V_{RL}}^2 + \qquad 0$$

COMPARISON OF CMOS AND NEMS LOGIC

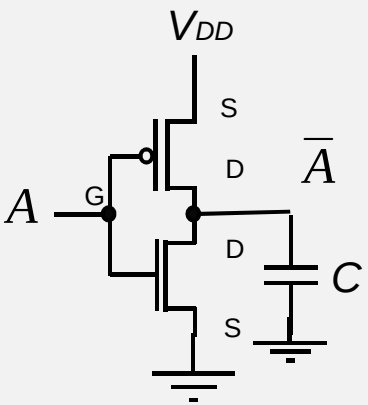


Strong effect of contact resistance

Contact technology is challenging

- Limits of CMOS
- Adiabatic solutions
- Capacitor Based Adiabatic solutions

Constant supply voltage

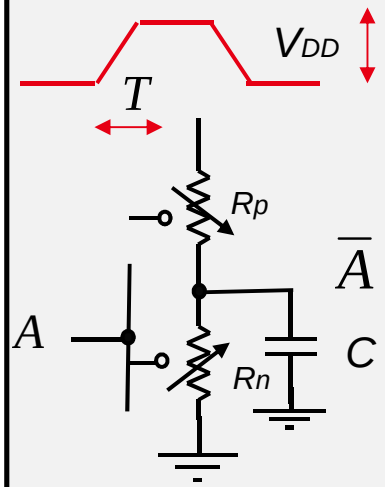


Conventional CMOS

$$E = \frac{1}{2} C V_{DD}^2$$

Leakage

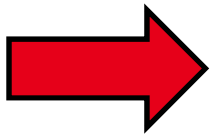
Variable supply voltage



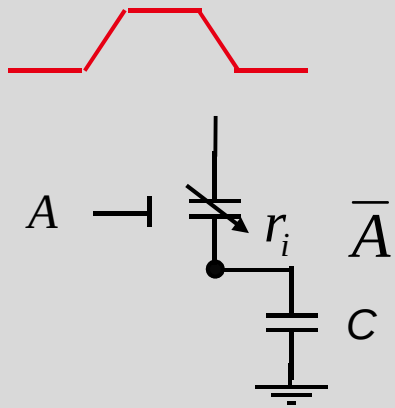
Adiabatic CMOS

$$E = \frac{R_P C}{T} C V_{DD}^2 + C V_T^2$$

Leakage



Variable supply voltage

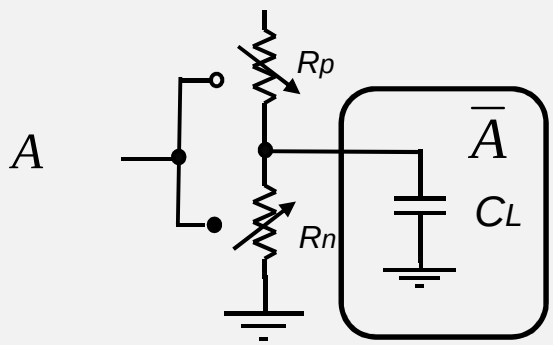


Adiabatic

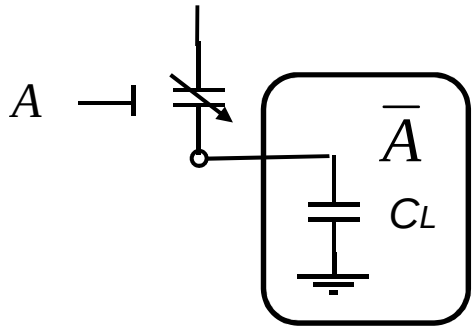
Capacitor based Logic

$$E = \frac{r_i C}{T} C V_{DD}^2$$

Zero leakage



$$V_s(t) = \frac{R_n(t)}{R_n(t) + R_p(t)} V_{DD}(t)$$



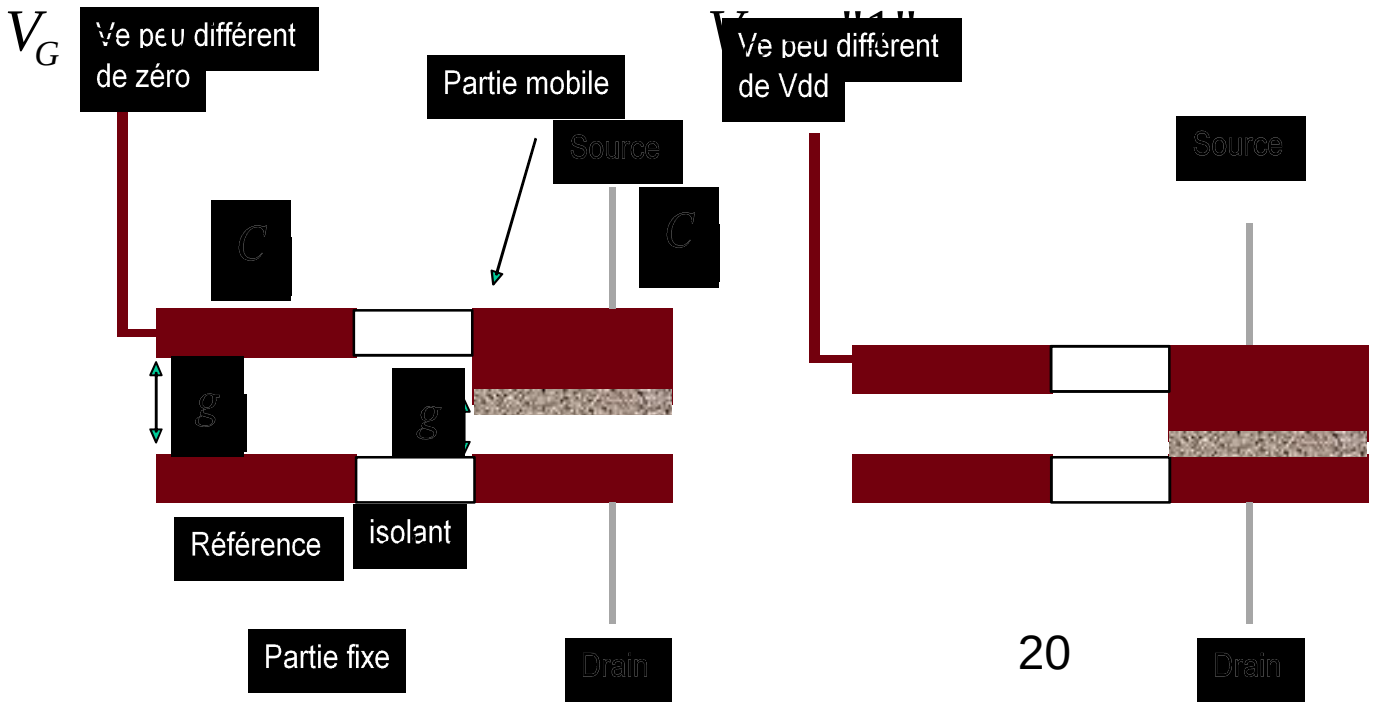
$$C\frac{d(V_{DD} - V_S)}{dt} + (V_{DD} - V_S)\frac{dC}{dt} = C_L \frac{dV_s}{dt}$$

$$\frac{d}{dt}(CV_{DD}) = -\frac{d}{dt}(C_L V_S) + \frac{d}{dt}(CV_S)$$

$$V_s(t) = \frac{C(t)}{C(t) + C_L} V_{DD}(t)$$

- Electrode geometry variation
- Permitivity variation

Microcapacitor example



CONCLUSIONS

- Adiabatic principle is « the » solution for ultra low power
- Reversible logic not necessary in a first step
- Choice of technology not yet clear but capacitor based logic seems promising